REMARKS

The undersigned attorney thanks Examiner Dang for his careful review of this patent application. Prior to entry of this amendment, claims 1 -25 were pending in the application. Claims 10 - 13 have been amended. Upon entry of this amendment, claims 1 - 25 will be pending.

Claims 13 – 15 and 18 Are Allowable Over the Cited References

In paragraph 1, the Office Action rejected claims 13 – 15 and 18 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Published Patent Application Publication No. 2002/0197844 to Johnson et al. (hereinafter "*Johnson*") in view of U.S. Patent Application Publication No. 2003/0107067 to Gudesen (hereinafter "*Gudesen*"). The rejection is respectfully traversed.

Johnson describes a method for making RF integrated circuit passive devices, which are compatible with copper interconnect metallization. An insulation layer is deposited upon an IC wafer, which includes the bottom half of an electronic component, such as a stacked spiral inductor, a capacitor, or a contact point. Next, a dielectric layer is deposited on the insulation layer to form a first insulator layer. A relatively thin resistive metal layer is then deposited on the first dielectric insulator layer. The thin metal layer may be optionally capped with a thin dielectric capping layer before the thin metal layer is patterned and etched to protect the thin metal layer during processing. Once the thin metal layer is etched, an optional second dielectric layer may be formed over the etched thin metal layer. Next, a relatively thick second insulator layer is formed over the structure. The thick second insulator layer is then masked and etched down to the top of the thin metal layer to define single damascene trenches. The trenches are then filled with a metal, which is preferably copper in conjunction with a copper barrier diffusion metal layer to coat the sides and bottom of the trenches. If aluminum or an aluminum alloy is used to fill the trenches, then the barrier metal layer is omitted.

Gudensen describes a structure for an integrated transistor/memory device. A source electrode and a drain electrode are positioned on a substrate of semiconducting material, which has been doped to form a source region, an ultra short transistor channel and a drain region. A memory material is then deposited on top of the semiconducting material in the form of a thin

layer of a polarizable dielectric material, which is capable of exhibiting hysteresis. The memory material is known in the art as a ferroelectric polymer or copolymer. The memory material fills the recesses between the source and drain electrodes and covers the top surface thereof to provide a barrier to the gate electrode.

The invention of Claim 13 of the present invention, describes a ferroelectric polymer die, which consists of a silicon (Si) substrate. On oxide thermal insulation layer is placed on top of the Si substrate and then a first metal layer is deposited on top of the oxide layer. Next, a ferroelectric polymer layer is deposited on top of the first metal layer. An interlevel dielectric (ILD) layer is then placed on top of the ferroelectric polymer layer. The die also contains a second metal layer, which is deposited on top of the ILD layer. The first metal layer and the second metal layer are electrically connected with a via fill plug, which passes through the ILD layer and the ferroelectric polymer layer.

Each and every element of the claimed invention, and well as a motivation or suggestion to combine the elements, must be found in the references to establish a *prima facie* case of obviousness. MPEP §2142. Neither *Johnson* or *Gudensen* describe, teach, or suggest, a ferroelectric polymer die having two metallization layers, as described by Claim 13. The Office Action stated that the metal layer (99) as described by *Johnson*, is broadly interpreted as a via metal plug because it is formed in the via. However, the element (99) described by *Johnson* is a copper diffusion barrier, which is well known in the art to be used with copper interconnects to prevent copper corrosion and interdiffusion. The trenches, or vias described by *Johnson* are "completely filled with metal, preferably copper *in conjunction with* a barrier metal." (Emphasis added). *Johnson*, pg. 5, para. 67. Therefore, the copper diffusion barrier is only part of the via plug. The copper plug if used by itself may degrade adhesion at the polymer/copper conductor interface, especially under conditions of high-humidity and high-temperature processing of subsequent layers. Furthermore, the copper plug may dissolve into the interfacial region of the polymer layer prior to curing, and adversely affects the dielectric and mechanical properties of the polymer layer to an unacceptable degree. Therefore, the trench plug is made of the copper fill metal (40) *in conjunction* with the copper diffusion barrier (99). The copper diffusion barrier is designed to prevent any interaction between the copper via plug and the polymer substrate and not to provide an electrical contact between the thin metal layer and the copper plug.

In addition, the ferroelectric die described by *Johnson* does not include a second metal layer on top of the ILD layer. Rather the copper plug, which the Office Action broadly interpreted as a second metal layer, lies entirely within the trench, or via. None of the copper plug lies outside the trench and none of the copper lies on top of the insulator layer. In fact, *Johnson* described removing all metal, both from the copper plug and the copper diffusion barrier, from the top of the insulator layer. "Following a conventional damascene process, a CMP removes the excess of the copper and any barrier metal layer from outside the trench shapes 42, 44, 46 so that only the trench shapes 42, 44, 46 are left filled with copper shapes 40, 46, 48, respectively, while the surrounding field is cleared of copper and barrier metal." *Johnson*, pg. 5, para. 70. Therefore, the copper plug, as described by *Johnson*, is a configured as a plug and not as a second metal layer that lies on top of the ILD layer, as described by Claim 13. Thus, *Johnson* teaches away from the claimed invention by requiring all metal be removed from the top of the ILD layer.

Because none of the cited references describes, teaches, or suggests a via metal fill plug passing through the ILD layer and the ferroelectric polymer layer to electrically connect the first metal layer to the second metal layer that is deposited the of the ILD layer, it is respectfully .submitted that claim 13, and all claims that depend there from are patentable over the cited art and it is requested that the rejection be removed and the claims be allowed to issuance.

Claims 10 -12 Are Allowable and In Condition for Allowance

Paragraph 2 of the Office Action rejected claims 10 – 12 under 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter. Specifically, the Office Action stated that the term "activation solution" in Claim 1 lacked antecedent basis. Similarly, the Office Action stated that the term "metal plating solution" of claim 1 lacked antecedent basis. The Office Action recommended that claim 10 and 11 should be amended to depend upon claim 5.

Claims 10 and 11 have been amended to now depend upon Claim 5. Therefore, claims 10 and 11 are now in condition for allowance and it is respectfully requested that the rejection of claim 10 and 11 be withdrawn and that claim 10 and 11 be passed onto issuance.

The Office Action also stated that the term "open area in the photoresist" lacked antecedent basis. Claim 12 has been amended to provide an antecedent basis. It is respectfully

submitted that Claim 12 is in condition for allowance and it is requested that the rejection of Claim 12 be withdrawn.

CONCLUSION

It is respectfully submitted that claims 1 - 25 are in condition for allowance and that each point raised in the Official Action with regard to these claims has been fully addressed. Therefore, it is respectfully requested that the rejections to claims 10 - 13 be withdrawn and that claims 1 - 25 be processed to issuance in accordance with Patent Office Business.

If the Examiner believes that there are any issues that can be resolved by a telephone conference, or that there are any informalities that can be corrected by an Examiner's amendment, please contact John Briski at 404.885.3141.

Respectfully submitted,

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